P-Channel 60-V (D-S) 175°C MOSFET

CHARACTERISTICS

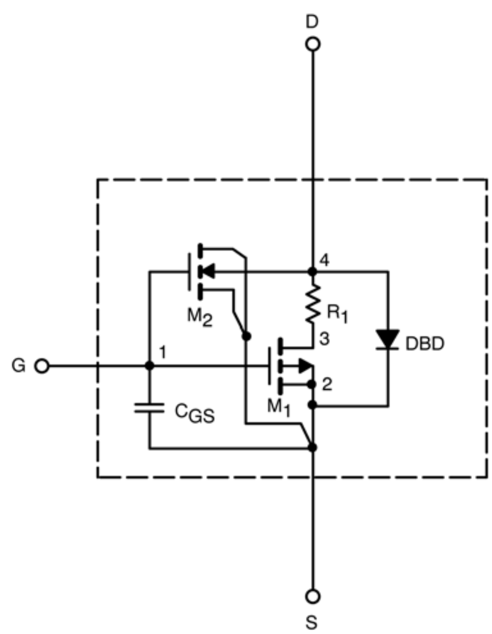
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

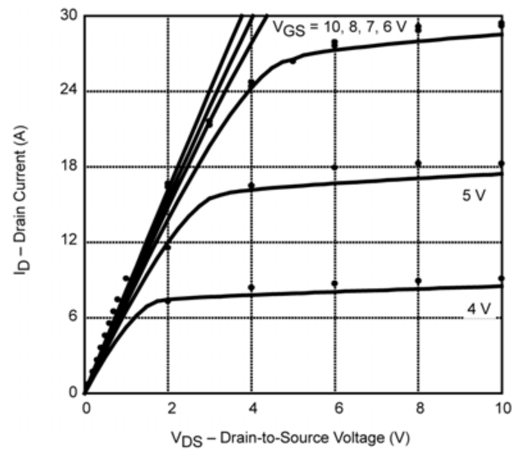


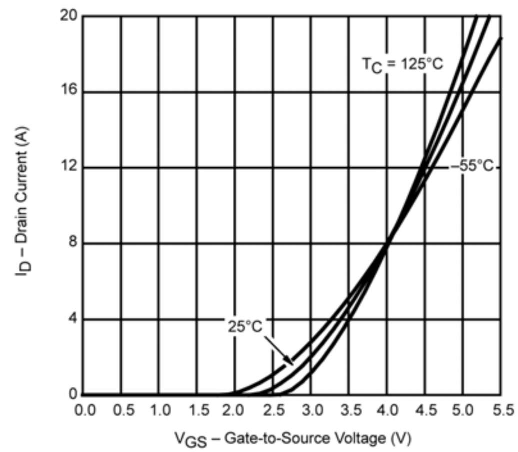
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

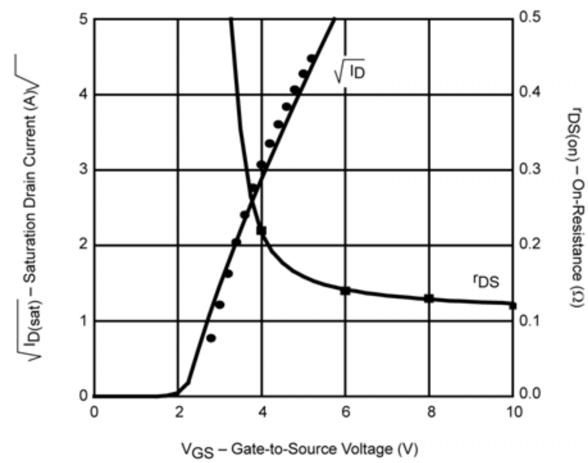
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250 µA	1.8		V
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –10 V	39		A
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –5 A	0.123	0.125	Ω
		V_{GS} = –10 V, I_D = –5 A, T_J = 125°C	0.21		
		V_{GS} = –10 V, I_D = –5 A, T_J = 175°C	0.26		
		V_{GS} = –4.5 V, I_D = –2 A	0.155	0.158	
Forward Transconductance [a]	g_{fs}	V_{DS} = –15 V, I_D = –5 A	7	8	S
Diode Forward Voltage [a]	V_{SD}	I_S = –2 A, V_{GS} = 0 V	–0.81	–0.90	V
Dynamic [b]					
Input Capacitance	C_{iss}	V_{DS} = –25 V, V_{GS} = 0 V, f = 1 MHz	562	450	nC
Output Capacitance	C_{oss}		63	65	
Reverse Transfer Capacitance	C_{rss}		34	40	
Total Gate Charge [c]	Q_g	V_{DS} = –30 V, V_{GS} = –10 V, I_D = –8.4 A	10	12.5	nC
Gate-Source Charge [c]	Q_{gs}		2.3	2.3	
Gate-Drain Charge [c]	Q_{gd}		3.2	3.2	

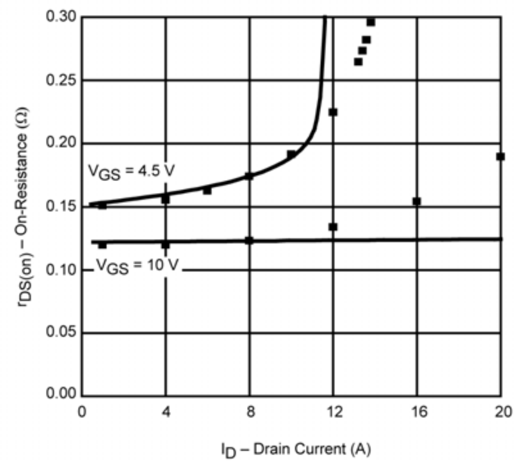
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

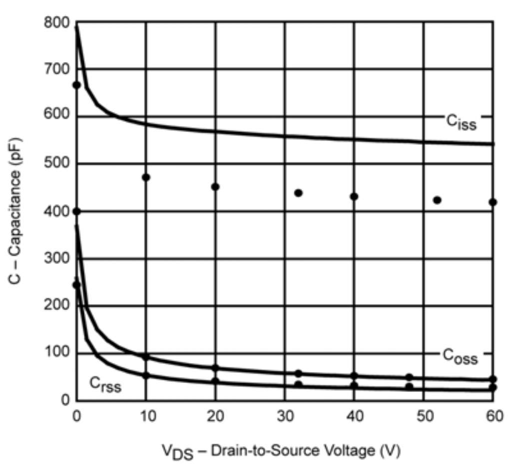
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

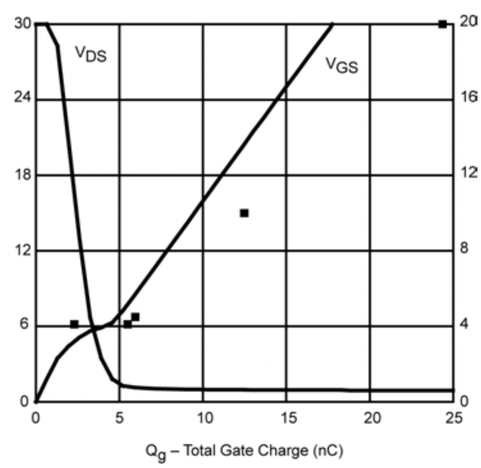












Note: Dots and squares represent measured data.

Disclaimer

All product specifications and data are subject to change without notice.

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